SOURCE SYNCHRONOUS CDMA BUS INTERFACE

ABSTRACT OF THE DISCLOSURE

A wireless IC interconnect system and a source synchronous CDMA (SS-CDMA) bus interface facilitate interconnections between first and second IC locations. A signal conveyed using the wireless system is modulated and capacitively coupled to a transmission medium, and then capacitively coupled from the medium to a receiver which demodulates the modulated signal and provides the demodulated signal to the second IC location. Multiple signals can be conveyed simultaneously by modulating and demodulating them using multiple access algorithms such as CDMA and/or FDMA. The SS-CDMA bus interface utilizes source synchronous signaling and CDMA techniques to provide high bus concurrency and low channel latency. The interface is re-configurable, and provides multi-chip access in high-bandwidth multi-drop parallel interconnection applications. The interface employs spread spectrum multiple access schemes, which enable two or more data bits to be sent through the same channel simultaneously and successfully recovered at the receiver.